Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (currently amended) A differential frequency doubler circuit, comprising:

differential input terminals;

differential output terminals;

a frequency doubler module coupled between said differential input terminals and a first one of said differential output terminals; and

a phase reversal module coupled between said frequency doubler module and a second one of said differential output terminals[[.]];

wherein said frequency doubler module includes first and second transistors with approximately equivalent width/length ratios; and

wherein said phase reversal module includes a third transistor with a width/length ratio approximately double said width/length ratios of said first and second transistors.

2. (original) The apparatus according to claim 1, wherein said frequency doubler module receives a differential input signal and generates a first output signal having a frequency that is double a frequency of the differential input signal, and wherein said phase reversal module generates a second output signal that is substantially equal in amplitude and opposite in phase to the first output signal,

wherein said first and second output signals form a differential output signal having the frequency that is double a frequency of the differential input signal.

3. (original) The apparatus according to claim 2, wherein said differential output signal has a duty ratio that is substantially equal to a duty ratio of the input signal.

4. (currently amended) The apparatus according to claim 1, wherein said ~~phase reversal module comprises a~~ third transistor ~~including~~ comprises a gate terminal coupled to a fixed voltage and a source terminal having a source terminal voltage that varies with an output of said frequency doubler.

5. (currently amended) ~~The apparatus according to claim 1,~~A differential frequency doubler circuit, comprising:

differential input terminals;

differential output terminals;

a frequency doubler module coupled between said differential input terminals and a first one of said differential output terminals; and

a phase reversal module coupled between said frequency doubler module and a second one of said differential output terminals;

wherein said phase reversal module comprises a transistor including a source terminal coupled to a fixed voltage and a gate terminal having a gate terminal voltage that varies with an output of said frequency doubler.

6. (original) The apparatus according to claim 1, further comprising:

a DC bias module coupled between said frequency doubler module and said phase reversal module.

7. (currently amended) The apparatus according to claim 1, wherein

said ~~frequency doubler module~~ first transistor comprises a first NMOS transistor including a gate terminal coupled to a first one of said differential input terminals, a drain terminal coupled to said first one of said differential output terminals, and a source terminal; and

[[a]] said second transistor comprises a second NMOS transistor including a gate terminal coupled to a second one of said differential input terminals, a drain terminal coupled to said first one of said differential output terminals, and a source terminal coupled to said first NMOS transistor source terminal; and

~~wherein~~ said ~~phase reversal module~~ third transistor comprises a third NMOS transistor including a drain terminal coupled to a second one of said differential output terminals, and a source terminal coupled to said source terminals of said first and second NMOS transistors, and a gate terminal coupled to said fixed voltage.

8. (original) The apparatus according to claim 5, wherein said frequency doubler module comprises:

a first NMOS transistor including a gate terminal coupled to a first one of said differential input terminals, a drain terminal coupled to said first one of said differential output terminals, and a source terminal; and

a second NMOS transistor including a gate terminal coupled to a second one of said differential input terminals, a drain terminal coupled to said first one of said differential output terminals, and a source terminal coupled to said first NMOS source terminal;

wherein said phase reversal module transistor comprises:

a third NMOS transistor including a drain terminal coupled to a second one of said differential output terminals, a source terminal coupled to said source terminals of said first and second NMOS transistors, and a gate terminal;

a differential amplifier including an output coupled to said gate terminal of said third NMOS transistor, said differential amplifier including a negative input coupled to said source terminals of said first, second, and third NMOS transistors; and

a fourth NMOS transistor including a gate terminal coupled to said fixed voltage, and a source terminal coupled to a positive input of said differential amplifier.

9. (currently amended) The apparatus according to claim [[7]]8, wherein a width/length ratio of said third NMOS transistor is approximately double a width/length ratio of said first and second NMOS transistors.

10. (currently amended) The apparatus according to claim 8, wherein a width/length ratio of said ~~third~~ fourth NMOS transistor is approximately ~~double~~ equal to a width/length ratio of said first[[,]] and second~~, and third~~ NMOS transistors.

11. (currently amended) A method of differentially doubling a frequency, comprising:

(1) receiving a differential signal having a first frequency;

(2) generating a first output signal from the received differential signal, the first output signal having a frequency that is double the first frequency;

(3) ~~generating a second output signal from the first output signal, wherein~~ controlling a transistor to receive the first output signal and generate a second output signal that is opposite in phase to the first output signal, including:

coupling a source terminal of the transistor to a fixed voltage;

varying a gate terminal of the transistor with the first output signal;

whereby the transistor generates the second output signal ~~is~~ substantially equal in amplitude and opposite in phase to the first output signal, wherein said first and second output signals form a differential output signal having a duty ratio that is substantially equal to a duty ratio of the received differential signal.

12. (cancelled)

13. (cancelled)

14. (currently amended) The method according to claim 1[[3]]1, wherein the varying of the gate terminal comprises varying a gate terminal of the transistor under control of an operational amplifier in a feedback loop.